

IN THE SPECIFICATION

Please replace paragraph [0012] with the following amended paragraph:

In one embodiment, the processor may be in communication with one another via an interconnect such as a bus 113. This bus 113 may also enable communication between the subcomponents of the processors such as caches in each processor. In another embodiment, any other type of communication interconnect may be utilized in place of or in conjunction with bus 113. The processors may also be in communication with a memory controller 115. Memory controller 115 may facilitate the reading and writing of data and instructions to system memory 121. Memory controller 115 may also facilitate communication with graphics processor 119. In another embodiment, graphics processor 119 may communicate with the processors via bus 113 or may be an input output (I/O) device 129/125 that communicates with the processors via bridges 117 and 123. Graphics processor 119 may be connected to a display device such as a cathode ray tube (CRT), liquid crystal display (LCD), plasma display device or similar display device. In one embodiment, the components connected to bus 113 may communicate with other system components on bus 131 or 135 through bridges 117 and 123. I/O devices 129 and 125 may be connected to the computer system through busses 131 and 135 and bridges 117 and 123. I/O devices 129 and ~~135-125~~ may include communication devices such as network cards, modems, wireless devices and similar communication devices, peripheral input devices, peripheral output devices such as printers, display devices and similar output devices, and other I/O devices that may be similarly connected to the computer system. Storage devices such as fixed disks, removable media readers, magnetic disks, optical disks, tape devices, and similar storage devices may also be connected to the computer system.

Please replace paragraph [0022] with the following amended paragraph:

In one embodiment, the exclusive volatile state may indicate the content of the cache line 203 is shared with another processor or device and the associated processor or device has ownership. The exclusive volatile state may include status information that identifies that some segment of cache line 203 may be in a volatile state and that some other segment of cache line 203 may be in a non-volatile state. In another embodiment, an exclusive volatile state may not be used.

Please replace paragraph [0050] with the following amended paragraph:

The volatile state system including supporting instructions may be implemented in software, for example, in a simulator, emulator or similar software. A software implementation may include a microcode implementation. A software implementation may be stored on a machine readable medium. A "machine readable" medium may include any medium that can store or transfer information. Examples of a machine readable medium include a ROM, a floppy diskette, a CD-ROM, an optical disk, a hard disk, ~~a radio frequency (RF) link~~, and similar media and mediums.